

BEST AVAILABLE COPY

PTO/SB/08A (10-01)

Approved for use through 10/31/2002. OMB 0851-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application Number	10/626718
		Filing Date	July 25, 2003
		First Named Inventor	MIURA et al.
		Art Unit	Unassigned 2818
		Examiner Name	Unassigned LONG TRAN
Sheet 1 of 1	Attorney Docket Number	300.33045CC3	

U.S. PATENT DOCUMENTS						
Examiner Initials ¹	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)				
UET		US-4,839,306		06/1989	Wakamatsu	
UET		US-4,842,675		06/1989	Chapman et al.	
UET		US-4,860,070		08/1989	Arimoto et al.	
UET		US-4,890,147		12/1989	Teng et al.	
UET		US-5,079,181		01/1992	Shimizu et al.	
UET		US-5,258,332		11/1993	Horioka et al.	
UET		US-5,293,512		03/1994	Nishigori et al.	
UET		US-5,298,782		05/1994	Sundaresan	
UET		US-5,329,138		07/1994	Mitani et al.	
UET		US-5,332,683		07/1994	Miyashita et al.	
UET		US-5,386,131		01/1995	Sato	
UET		US-5,428,239		06/1995	Okumura et al.	
UET		US-5,461,248		10/1995	Jun	

FOREIGN PATENT DOCUMENTS							
Examiner Initials ¹	Cite No. ¹	Foreign Patent Document		Publication Date MM-DD-YYYY	Country	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ³
		Country Code ² -Number ⁴ -Kind Code ⁵ (if known)					
UET		JP	3-96249	04/1991	Japan (Abstract only)		
UET		JP	3-236283	10/1991	Japan		
UET		JP	4-127433	04/1992	Japan (Abstract only)		

OTHER DOCUMENTS	
Miura et al., "Residual Stress Measurement in Silicon Substrates after Thermal Oxidation", JSME Int'l Journal, Series A, Vol. 36, No. 3, 1993, pages 302-308	
Wolf, "Fully Recessed Oxide Locos Processes", Silicon Processing for the VLSI Era, Vol. II, page 28, 2.3	
Saito et al., "Development of a Stress Simulation Program For Semiconductor Devices Considering Their Fabricating Process", Computational Mechanics '91 Proc. of Int. Conf. on Comp. Eng. Sci. 1991, pages 880-883	
Saito et al., "A Two-Dimensional Thermal Oxidation Simulator Using Visco-Elastic Stress Analysis", IEDM, 1989, pages 695-698	
Magdo et al., "Framed Recess Oxide Scheme For Dislocation-Free Planar Si Structures", SOLID-STATE SCIENCE AND TECHNOLOGY, Vol. 125, No. 6, 1978, pages 932-936	
Chiu et al., "A Bird's Beak Free Local Oxidation Technology Feasible for VLSI Circuits Fabrication", IEEE TRANSACTIONS ON ELECTRON DEVICES, Vol. ED-29, No. 4, 1983, pages 536-540	

Examiner Signature	LONG TRAN	Date Considered	11/01/04
--------------------	-----------	-----------------	----------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³Enter Office that issued the document, by the two-letter code (WIPO Standard St.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.